

**Digital Logic Lab Assignment # 3**

**3.**To verify the operation of 3 input AND

and OR gate using sinle gate

# Submitted By

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**Year/SEM : 2017/1st Semester**

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# Submitted To

|  |  |  |
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**OBJECTIVE 3.1:**

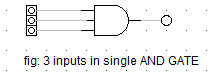
**TO VERIFY THE OPERATION OF 3 INPUT AND GATE USING SINGLE GATE .**

**THEORY:**

The AND gate is a basic digital [logic gate](https://en.wikipedia.org/wiki/Logic_gate) that implements [logical conjunction](https://en.wikipedia.org/wiki/Logical_conjunction).A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If neither or only one input or only two inputs to the AND gate is HIGH(1), a LOW(0) output results.

**Boolean expression: F= (A.B.C)**

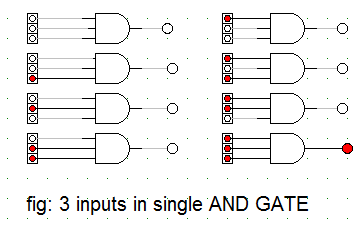
**CIRCUIT DIAGRAM:**

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**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUTS** | | | **OUTPUT** |
| **A** | **B** | **C** | **(A.B.C)** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** |

**OBSERVATION:**

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**OBSERVATION TABLE:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **INPUTS** |  |  | | **OUTPUT** |
| **A** |  | **B** | | **C** | **(A.B.C)** |
| **0** |  | **0** | | **0** | **0** |
| **0** |  | **0** | | **1** | **0** |
| **0** |  | **1** | | **0** | **0** |
| **0** |  | **1** | | **1** | **0** |
| **1** |  | **0** | | **0** | **0** |
| **1** |  | **0** | | **1** | **0** |
| **1** |  | **1** | | **0** | **0** |
| **1** |  | **1** | | **1** | **1** |

**CONCLUSION:**

Hence, the property of AND gate was verified.

**REFERENCE:**

**http://www.physicshandbook.com/top/topicc/combgates.htm**

**OBJECTIVE 3.2:**

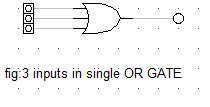
**TO VERIFY THE OPERATION OF 3 INPUT OR GATE USING SINGLE GATE .**

**THEORY**

The OR gate is a digital [logic gate](https://en.wikipedia.org/wiki/Logic_gate) that implements [logical disjunction](https://en.wikipedia.org/wiki/Logical_disjunction). A HIGH output (1) results if one ,two or all the inputs to the gate are HIGH (1). If neither input is high, a LOW output (0) results.

Boolean expression: F= (A+B+C))

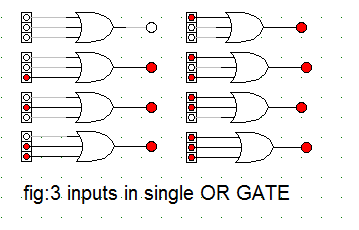
CIRCUIT DIAGRAM:

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**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUTS** | | | **OUTPUTS** |
| **A** | **B** | **C** | **(A+B+C)** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

**OBSERVATION:**

**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUTS** | | | **OUTPUTS** |
| **A** | **B** | **C** | **(A+B+C)** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** |
| **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

**CONCLUSION:**

Hence, the property of OR GATE was verified.

**REFERENCE:**

**http://www.physicshandbook.com/top/topicc/combgates.htm**